Performance Evaluation of GaN based PFC Boost Rectifiers

Srinivas Harshal, Vijit Dubey

Abstract - The power electronics industry is slowly moving towards wideband semiconductor devices such as SiC and GaN but not without facing challenges such as relatively limited device knowhow, scarce driver support technology and per unit cost. This paper aims to evaluate performance improvements using GaN FET’s, if any, in conventional boost and interleaved boost PFC rectifier topologies thereby making an engineering and economic case for its widespread use in high power applications. Design considerations and choice of topology based on different power levels are discussed for CCM operation and closed loop control is implemented. Design examples and simulation results are shown for comparison with silicon devices using a representative topology from the boost/interleaved PFC family.

Keywords – Boost PFC; Interleaved PFC; GaN based PFC; Closed loop Control, PLECS Thermal modeling, Double pulse Testing.

I. INTRODUCTION

Wide band-gap devices such as SiC and GaN enable switching power supplies take advantages of the high frequency operation at high efficiencies as shown in Figure 1.

In this paper a cost to efficiency and volume analysis for GaN FET’s against their traditional Si counterparts for the most common PFC topologies is given. Ultra-fast recovery SiC diodes are used in all the topologies discussed in this paper in order to draw attention only to the differences, benefits or drawbacks of PFC topologies solely based on FET choices. It follows that IGBT based PFC circuits are not discussed and power levels are restricted to 1kW.

DCM operation has the highest peak current compared to CrCM or CCM, and this study will focus on CCM operation for high power levels. Although CrCM boost has advantages of power density, at high power levels a premium for low filtering and high peak current has to be paid. Hence, a CCM is a better choice. [2]

II. DEVICE MODELING IN PLECS

For modeling the devices – GaN, MOSFET and SiC, Relavent datasheets are used to determine device characteristics. Key data points for thermal modeling in PLECS include the turn on and turn off characteristics for switching loss and Rds on for Conduction loss. This information is usually unavailable directly and hence a test circuit for double pulse inductive load switching is built in SPICE using device manufacturer’s models to obtained the Switching energy loss. Sample double pulse test circuit for GaN Systems 650V device is shown in following figure.
The choice of the devices for boost PFC is as follows:

- **Si MOSFET**: Infineon CoolMOS C7 IPW65R045C7
- **GaN FET**: GaN Systems G66508-B
- **SiC diode**: 5TH Gen Thin-Q IDK10G65C5
- **Inductor**: Torroidal CoolMu Core from Magnetics Inc. wound with Gauge 13 copper wire.

It is worth noting that the Rds on for CoolMOS and GaN Systems FET are almost same but the switching times are dramatically lower for GaN Systems which gives us higher efficiencies at high power and chance to increase frequency of the Boost PFC without affecting the junction temperatures.

Their thermal characteristics are modelled into PLECS as shown in following figures.

![Figure 3 Double pulse Test](image)

![Figure 4 Infineon CoolMOS turn on and turn off characteristics](image)

![Figure 5 GaN turn on and turn off characteristics](image)

![Figure 6 Infineon CoolMOS Conduction Characteristics](image)

![Figure 7 SiC Boost Diode Conduction Characteristics](image)

### III. BOOST PFC DESIGN

This is the most common topology for PFC applications. In PFC applications, a diode bridge is used to rectify the ac input voltage to dc, and this is fed to a boost converter, as shown in Fig. 8. However, the output capacitor ripple current is very high. Also, as the power level increases to a few hundred watts, the diode bridge losses affect the efficiency, and heat sink design is complicated.

The converters which are designed in this project are based on the following specifications which can serve data centers or Electric Vehicle chargers a:

- Input voltage range: 90V - 220V (nominal 120V)
- Output voltage range: 400V
- Output Power (Full load): 1kW
- Switching frequency: 100khz;
- Objective: 90% and above efficiency, 1% Output Voltage Ripple, Less than 3% THD
A. Power Stage

The boost inductor is calculated as follows:

\[
L = \frac{1}{\%\text{Ripple}} \cdot \left(\frac{V_{a,c,min}}{P_0}\right)^2 \left(1 - \sqrt{2} \cdot \frac{V_{a,c,min}}{V_o}\right)
\]

The capacitor has the following considerations

\[
C_o \geq \frac{2 \cdot P_0 \cdot t_{\text{hold}}}{V_o^2 - V_{o,min}^2}
\]

\[
C_o \geq \frac{P_0}{2 \cdot \pi \cdot f_{\text{line}} \cdot \Delta V_o \cdot V_o}
\]

\[
\text{ESR} = \frac{DF}{2 \cdot \pi \cdot f \cdot C_o}
\]

Following the design procedure,

\(L_r\) comes out to be = 230\(\mu\)H

\(C_r\) comes out to be = 770\(\mu\)F

The switching and conduction losses in the FET can be estimated as follows.

\[
P_{S,\text{on}} = 0.5 \cdot I_{\text{avg}} \cdot V_o \cdot t_{\text{on}} \cdot f
\]

\[
P_{S,\text{off}} = 0.5 \cdot I_{\text{avg}} \cdot V_o \cdot t_{\text{off}} \cdot f
\]

\[
P_{S,\text{cond}} = I_{\text{rms}}^2 \cdot R_{\text{on}}
\]

The simulation results can be seen in figures 9 through 12 where input current is sinusoidal, THD is low and the junction temperatures do not exceed permitted value of 150 deg. C.
**B. Closed loop control implementation**

The continuous input current is forced to track changes in output voltage by average current mode control technique. Implementation is shown in figures 13 through 15 and results for Dynamic load step change in figure 16. The Loop gains are shown in figures 17 and 18.
C. Performance improvement using GaN

All other things considered same, maximum efficiency can be seen to have been improved in Figure 19 by 1.9%. (Blue curve)

![Figure 19 Efficiency comparison for Boost PFC](image)

This translates to about 19W but the unit cost price for GaN FET is around 12 USD while The Infineon CoolMOS costs around 8.75 USD. While this might be too high a price to pay for such reduced gains real benefits of using GaN are not realized until the switching frequency is increased to 150kHz.

At this increased frequency the Max. Efficiency is does not get affected greatly (Converter is still about 95.3% Efficient) despite considerable switching losses at such high frequency. However, the size of the Torroidal inductor drops by 389 sq.mm. This also results in reduced input EMI filter sizing whose gains in area are not quantified in this paper. The bill of Materials for main components are shown in the presentation to further support the claim that volumetric efficiencies can justify the increased price.

IV. INTERLEAVED BOOST PFC DESIGN

In the Boost PFC topology the change in inductor ripple current, appears at the converter's input and thus requires filtering to comply with EMI regulation. Furthermore, the current from the boost diode has a high ripple compared to the average dc output current. This results in a larger capacitor value. These are mitigated using an intereaved boost PFC.

![Figure 20 Interleaved Boost converter](image)

![Figure 21 Interleaved Boost converter](image)

D. Power Stage

The designed values for L & C for a 1kW application are shown below. The schematic for is shown in fig. 22.

![Figure 22 Interleaved Boost converter](image)
The mains RMS is reduced and is given by the formula

\[ I_{M.rms} = \frac{P_{out}}{\sqrt{3} \cdot \eta \cdot V_{ac.ll}} \cdot \sqrt{1 - \frac{8\sqrt{2} \cdot V_{ac.ll}}{3 \cdot \pi \cdot V_{ac.ll}}} \]

Following figure shows the input current waveform.

![Figure 23 Interleaved Boost Converter Input Current](image)

The devices for interleaved boost are chosen as follows:

Si MOSFET : Infineon CoolMOS C7 IPA65R190C7

GaN FET : GaN Systems GS66502B

SiC diode : 5TH Gen Thin-Q IDH05G65C5

Capacitor RMS currents and Inductor RMS currents are reduced after interleaving and they are governed by the following equations respectively.

\[ I_{C.out,rms} = \sqrt{\frac{16 \cdot \sqrt{2} \cdot P_{out}^2}{9 \cdot \pi \cdot V_{ac.ll} \cdot V_{out} \cdot \eta} - \left(\frac{P_{out}}{V_{out}}\right)^2} \]

\[ I_{l.rms.max} = \frac{P_{out} \cdot \sqrt{2}}{\eta \cdot V_{ac.ll} \cdot \sqrt{6}} \]

**E. Control Stage**

This voltage controller is a trans conductance type amplifier that is compensated. This generates a signal that is then shaped to the input sinusoidal voltage waveform. This quantity is then gained up and then fed to the current controller after subtracting from the respective inductor currents. The e current controller was designed using an OTA with external compensation networks. The output of this current controller is then fed to the PWM block that drives the two FET’s 180 degrees out of phase in the interleaved Boost PFC. Figure 24 and 25 Summarize the control action and response respectively.

![Figure 24 Interleaved Boost converter Control](image)

**F. Performance improvement with GaN**

The efficiency for a 1kW PFC is highest for an interleaved GaN PFC. However the gain is not as appreciable because the cost of the FET involved is substantial. If the design is driven by size definitely GaN is much advantageous for reduction of passives in the circuit with its high frequency operation.

![Figure 26 Efficiency – GaN vs CoolMOS (Solid and dotted Blue for interleaving, Solid and dotted Red for Boost)](image)
When consider bridge diode losses to be the same for both GaN and Si based PFC it is interesting to note that switching losses dominate the overall loss picture.

![Loss distribution- Interleaved CoolMOS(Blue), Interleaved GaN(Orange), Boost CoolMOS(Grey), Boost GaN(Yellow)](image)

**Table 1 Boost PFC – GaN vs CoolMOS**

<table>
<thead>
<tr>
<th></th>
<th>Boost PFC with Si MOSFET</th>
<th>Boost PFC with GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Levels</td>
<td>Low</td>
<td>Mid-High Range</td>
</tr>
<tr>
<td>Typical Efficiency</td>
<td>Lower at High Power</td>
<td>Higher than Boost at 1kW</td>
</tr>
<tr>
<td>Switching Loss</td>
<td>Higher</td>
<td>Around 90% less</td>
</tr>
<tr>
<td>Magnetic Volume</td>
<td>Typically large due to freq. limitations</td>
<td>Can be reduced with higher freq.</td>
</tr>
<tr>
<td>EMI/ Noise</td>
<td>Lower</td>
<td>Higher when Fsw Increased</td>
</tr>
<tr>
<td>Cost</td>
<td>Lower per unit</td>
<td>Much Higher</td>
</tr>
</tbody>
</table>

**Table 2 Interleaved Boost PFC – GaN vs CoolMOS**

<table>
<thead>
<tr>
<th></th>
<th>Boost PFC with Si MOSFET</th>
<th>Boost PFC with GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Levels</td>
<td>Mid Range</td>
<td>Mid-High Range</td>
</tr>
<tr>
<td>Typical Efficiency</td>
<td>Better at Higher Power</td>
<td>Higher than Si at 1kW</td>
</tr>
<tr>
<td>Switching Loss</td>
<td>Lower due to interleaving</td>
<td>Further reduced by interleaving</td>
</tr>
<tr>
<td>Conduction Loss</td>
<td>Lower due to interleaving</td>
<td>Similar to Si</td>
</tr>
<tr>
<td>Magnetic Volume</td>
<td>Very large due to freq. limitations</td>
<td>Improvements at higher freq.</td>
</tr>
<tr>
<td>EMI/ Noise</td>
<td>Lower</td>
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</tr>
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From table 1 and 2 we gather that the replacement of, with Si MOSFET with GaN affects the power density and efficiency of the PFC circuit in both boost and interleaved boost topologies. The size of passives in the circuit as well as Efficiency at high power levels (1kW), are improved. However, it is incumbent upon the designer to identify what drives the design – Cost or Size. For reduced EMI filter and boost inductor size using a GaN FET is beneficial but for a given frequency it is not justifiable economically.

**VI. FUTURE WORK**

No study is complete without hardware verification. As such, these simulation studies are only as good as the models used which are based on the manufacturer’s data. A prototype with the most suitable GaN FET’s (from a selection of available FET’s) to establish the results of this study will reinforce the arguments presented in this paper. A comprehensive study is in order for some given application – such as a telecom power supply or an Electric Vehicle charger as the results discussed in this paper are topology specific only and not application specific. Bridgeless PFC must be explored for this application as it significantly improves efficiency due to elimination of bridge diode losses.
VII. REFERENCES

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